Sandip Foundation's
Sandip Institute of Technology & Research Centre, Nashik
Department of Electronics & Telecommunication

**Date:** 17st March 2017

**Name of Event**:- Two Days workshop on "FPGA Based Digital system design using VHDL"

**Date of Event**:- 15-16 March. 2017

**Name of resource person**:- Dr. Sanjeev Sharma, Prof. M. P. Mahajan

**Objectives:** The objective of this workshop is to make students skillful in practical,projects and for industrial jobs by improving the knowledge of PLD such as FPGA,CPLD & its industrial applications.

**Contents Covered in the Workshop:**

**1)Introduction:-** The scope and application of VHDL
- Design and tool flow
- FPGAs
- The VHDL world

**2)Getting started:-**
- The basic VHDL language constructs
- Entities and Architectures
- Signals and Ports
- Sequential & Concurrent assignments
- VHDL source files and libraries
- The compilation procedure
- Synchronous design and timing constraints

**3)FPGA Design Flow :-**
- Simulation
- Synthesis
- Place-and-Route
- Device programming

**4)Synthesizing Combinational & Sequential Logic:**

**5) Finite state Machine design using VHDL**

**6)LCD & Keypad Interface**

**7) Practical exercises using a ALTERA DE0 & DE2 hardware board**

**Outcome: After successfully completing the workshop students will be able to**

1)Understand the importance , scope & application of VHDL & FPGA.

2)Model the digital circuit with VHDL,simulate,synthesize & prototype in PLD.

3)Design various application using ALTERA FPGA.

## Photos: